

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,891,213 B1
APPLICATION NO. : 10/626777
DATED : May 10, 2005
INVENTOR(S) : Wendell P. Noble

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Item (56), Line 1	“A SRAM memory cell”	--An SRAM memory cell--
Item (56), Line 11	“and has a reduced power”	--and has reduced power--
Column 1, Line 42	“for 1.5V”	--for 1.8V--
Column 2, Lines 23 and 60	“a NPN”	--an NPN--
Column 2, Line 60	“in FIG. 2, however,”	--in FIG. 2; however,--
Column 2, Lines 62 and 63	“a NMOS”	--an NMOS--
Column 3, Line 2	“340 N”	--34 ON--
Column 4, Line 25	“SRAM”	--SRAM of--
Column 4, Line 53	“with in the”	--within the--
Column 5, Line 8	“concentration NA”	--concentration N _A --
Column 5, Line 10	“is a”	--is an--
Column 5, Line 12	“concentration ND”	--concentration N _D --
Column 5, Line 16	“concentration NA of about 102°”	--concentration N _A of about 10 ²⁰ --
Column 6, Line 40	“exposed portions the”	--exposed portions of the--

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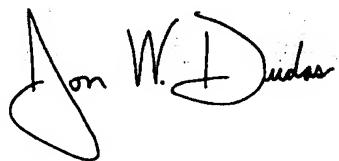
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<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Column 7, Line 38	"n+ type"	--n+-type--
Column 7, Line 41	"F squared"	--F ² --
Column 8, Line 17	"SRAM 175 FIG. 11,"	--SRAM 175 of FIG. 11,--

Signed and Sealed this

Thirteenth Day of March, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office